Unit 8: Combinational Circuit Design Using Gates

8.1 Review of Combinational Circuit Design

Steps

1. Setup a Truth Table
   A. For n variable inputs, 2^n rows

   B. Don't Cares for values that never occur

2. Derive a Simplified Algebraic Expression
   A. Karnaugh Maps

   B. Quine Mc-Cluskey

3. Realize the Circuit
   A. Levels / Gates

   B. Single / Multiple Output

4. Types.
   A. 2-Level
      1. AND-OR, NAND-NAND, OR-NAND, NOR-OR from minimum SOP

      2. OR-AND, NOR-NOR, AND-NOR, NAND-AND from minimum POS

   B. Multi-Level
      1. NAND
         a. Minimum SOP
         b. Output is OR
         c. AND outputs not AND inputs, OR outputs not OR inputs
         d. Replace AND's and OR's with NAND's
         e. Invert literals on odd Levels

      2. NOR
         a. Minimum POS
         b. Output is AND
         c. AND outputs not AND inputs, OR outputs not OR inputs
         d. Replace AND's and OR's with NOR's
         e. Invert literals on odd Levels

8.2 Design of Circuits with Limited Gate Fan-in

Fan-in: number of inputs on each gate. (May be limited, if a circuit requires more, factor)

Ex.

Note: When designing multilevel-output circuits it is best to minimize each function seperately then factor the expression to increase the levels recognizing common terms when possible.

8.3 Gate Delays and Timing Diagrams

Gate Delay: Time it takes a gate output to change when an input to as logic gate changes.

Notes: Gate delays for a 0 to 1 transition can differ from a 1 to 0

Very short gate delays can be ignored

Timing Diagram: Diagram where several variables of a function are plotted on the same time scale to observe the times at which the variables change with respect to one another.

8.4 Hazards in Combinational Logic

When a combinational circuit input changes, the output may experience unwanted switching transients

Static 1-hazard: When a single input change may cause the output to momentarily go to a 0 when it should remain a 1.

Static 0-hazard: When a single input change may cause the output to momentarily go to a 1 when it should remain a 0.

Dynamic hazard: When an output is supposed to change from a 0 to a 1 (or 1 to 0) but the output may change 3 or more times

Procedure for hazard detection in a two-level AND-OR circuit

1. Write the SOP expression for the circuit

2. Plot each term on a Karnaugh map and loop it.

3. If any two adjacent 1's are not covered by the same loop, a 1-hazard exists for the transition between the two 1's.

Procedure for circuit designs free of static or dynamic hazards

1. Find a SOP expression (F^t) for the output in which every pair of adjacent 1's is covered by a 1-term. (The sum of all prime implicants will always satisfy this condition). A two-level AND-OR circuit based on this F^t will be free of 1-, 0-, and dynamic hazards.

2. If a different form of the circuit is required, manipulate F^t to the desired form by simple factoring, DeMorgan's Law, etc. Treat each x_i and x_i' as independent variables to prevent introduction of hazards.

Note: By starting with the POS and looping 0's while following the above procedure will yield a hazard free OR-AND circuit.

8.5 Simulation and Testing of Logic Circuits

Simulation

- Verifies design and debugs a circuit
- Easier, faster, more economical than actually building
- Can be used to verify
    - Design is logically correct
    - Timing is correct
    - Tests for the circuit

Simple Simulator for Combinational Logic

1. Circuit inputs are applied to the first set of gates and the outputs are calculated

2. The outputs that are changed in step 1 are fed into the next level of gate inputs and the outputs of those gates calculated.

3. Step 2 repeated until no more changes in gate inputs occur. The circuit is then on steady-state and the outputs can be read.

4. Steps 1 – 3 are repeated every time a circuit input changes

<u>Four-Valued Logic</u> – to properly simulate a circuit 4 logic values are necessary 0, 1, X and Z. Where X represent an unknown value and Z represents an open circuit (no connection)

AND and OR functions for four-valued logic

·	0	1	X	Z
0	0	0	0	0
1	0	1	X	X
X	0	X	X	X
Z	0	X	X	X

+	0	1	X	Z
0	0	1	X	X
1	1	1	1	1
X	X	1	X	X
Z	X	1	X	X

Ex.

Possible Cause for incorrect circuit output

1 Incorrect design

2 Gates connected wrong

3 Wrong input signals to the circuit

(Additional if lab built)

4 Defective gates

5 Defective connecting wires